IN THE CLAIMS

Claims 1-10 and 15-23 were pending. Claims 1, 5, and 15 have been amended. Claims 6-7, 16, and 20-23 have been canceled without prejudice. Claims 1-5, 8-10, 15, and 17-19 remain pending. A complete list of claims is presented below with amendments marked up:

Current Listing of Claims

1. (Currently amended) A memory interface comprising:

an inductor;

a resistor coupled to the inductor in series; and

a plurality of transmission lines, coupled to the inductor in series, to couple a plurality of memory devices to a circuit board.

2. (Original) The memory interface of claim 1, further comprising:

one or more impedance transformers coupled to the inductor in series.

3. (Original) The memory interface of claim 2, wherein one or more of the plurality of transmission lines are used as the one or more impedance transformers.

4. (Original) The memory interface of claim 1, wherein the plurality of memory devices comprises one or more synchronous dynamic random access memories (SDRAMs) operable at a frequency above 200 MHz.

5. (Currently amended) A method to interface a circuit board with a plurality of memory devices, the method comprising:

coupling the plurality of memory devices to a semiconductor device by circuitry, the circuitry including an inductor and a resistor coupled to the inductor in series, wherein the circuitry is fabricated on the circuit board and the semiconductor device is a memory controller mounted on the circuit board.

6. (Canceled).

7. (Canceled).

8. (Original) The method of claim 5, wherein the circuitry comprises a plurality of transmission lines coupled to the inductor in series on the circuit board.

9. (Original) The method of claim 8, wherein the plurality of transmission lines comprises one or more impedance transformers.

10. (Original) The method of claim 5, wherein the plurality of memory devices includes one or more synchronous dynamic random access memories (SDRAMs) operable at a frequency above 200 MHz.

11.- 14. (Canceled).

15. (Currently amended) A computer system comprising:

a plurality of synchronous dynamic random access memories (SDRAMs);

a memory controller; and

a memory interface coupling the memory controller to the plurality of SDRAMs, the memory interface comprising

an inductor,

a resistor coupled to the inductor in series, and

a plurality of transmission lines coupled to the inductor.

16. (Canceled).

17. (Original) The computer system of claim 15, wherein the plurality of transmission lines includes one or more impedance transformers.

18. (Original) The computer system of claim 15, further comprising a processor coupled to the memory controller.

19. (Original) The computer system of claim 15, wherein the plurality of SDRAMs includes a double-data rate (DDR) SDRAM device.

20-26. (Canceled).